# Alessandro Renzi

*Curriculum Vitae*

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## Info

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|---|---|---|---|
| Born | January 7th, 1990 in Rimini (Italy) | Citizenship | Italian |
| Driver's License | Italian A and B | LinkedIn | `https://www.linkedin.com/in/alessandro-renzi-84b91a26/` |
| Website | `www.nullptr.it` | | |

## Desidered Employment and Current Skills

### Hardware Engineer - Digital Electronics

I have always been interested in both hardware and software and I study them since the third year of high school, going beyond the lessons by my own as much as possible. I'm looking for a job in architectural and RTL design possibly covering also software integration. I'm very good at mixing knowledge from different areas and always willing to learn new things, especially from people more experienced than me. I'm able to work without supervision but also as part of a team.

## Technical skills

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|---|---|
| Programming Languages | C/C++, Verilog, SystemVerilog, VHDL, SystemC, Assembly, C#, Java, Bash, Python, TCL, Makefile, Latex |
| CAD Tools | Synopsys DesignCompiler, Synopsys Primetime, ModelSim, QuestaSim, Cadence JasperGold, Cadence Encounter, Cadence CtoS, Xilinx EDK, Multisim, Ultiboard, Eagle, AWR Microwave Office |
| Libraries & IDEs | OpenCV, OpenMP, Qt, Matlab, Simulink, Mathematica, LabView, Xilinx ISE, Altera QuartusII, MPLAB, CodeWarrior, mbed.org, Eclipse, QtCreator |
| Hardware Platforms | PIC16F, PIC18F, PIC24F, Xilinx ZYNQ 7000, Zedboard, Altera Cyclon II, Wiznet W5100 and W5200, WIZ820io, FRDM-KL25Z, MSP430 LaunchPad, RaspberryPi |
| Other | Linux, UML, Git, CMake, Doxygen, Jenkins, Gerrit, AMBA Protocols, AXI, AXI Stream, AHB, APB, CHI Bus Protocol, Arm Low Power Interface, Arm Distributed Translation Interface |

## Languages

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|---|---|
| Italian | **Native** |
| English | **Fluent** |

## Education

2012 - 2015 **Master Degree in Electronic Engineering**, *Polytechnic University of Turin*, Turin, Italy.
Specialization in Embedded Systems, **Grade:** 110/110, **GPA:** 3.67
Thesis links: Summary, Complete
Courses:

- **Codesign Methods and Tools**(30): Design a complex HW/SW system and model functions, parameters and data as methods and attributes of UML classes.
- **Computer Architectures**(25): Assembly programming techniques, pipeline processors, instruction level parallelism, compiler techniques, static and dynamic branch prediction, out of order execution, hardware based speculation, ARM architecture and AMBA bus fundamentals.
- **Electronic Systems Engineering**(30): Advanced PCB design, EMI.
- **Electronics for Embedded Systems**(28): Embedded systems, operational amplifiers, ADC and DAC, power electronics, memories, programmable logics, communication bus, CPU peripherals.
- **Guiding electromagnetic systems**(30): Microwave filters, circulators, power dividers, directional couplers, mixers, electromagnetic compatibility.
- **Integrated systems architecture**(30): Pipelining, retiming, folding, unfolding, algorithm transformation for ASIC implementation, architecture exploration, VLIW architectures, instruction level parallelism, arithmetic circuits, on-chip interconnections, network-on-chip.
- **Microelectronic systems**(30L): High level architectures case studies (Pentium4, Niagara T2, ARM), CPU's functional blocks (adders, multipliers, dividers, ALUs, Register files, etc.), VHDL implementation and synthesis laboratories (ST's 90 nm), logic families, physical design, post-layout verification.
- **Model-based software design**(30L): Model-based software design workflow, automotive case-study, ISO26262 standard, AUTOSAR, Misra C, Simulink algorithm modeling, automatic code generation, code integration on ARM platform.
- **Modeling and optimizations of embedded systems**(30): System level and RTL level modeling in SystemC, EFSM composition, control dominated system modeling in ECL (C Esterel), hardware and software synthesis of Esterel code and OS interfacing, formal verification, schedulation of dataflow network, Kahn process network and boolean dataflow network, dataflow network hardware synthesis, WCET (worst case execution time) analysis of software.
- **Operating systems**(30L): OS classification, kernel, process, process synchronization, process communication, threads, embedded OS, development tool chain, system programming through POSIX APIs.
- **Synthesis and optimization of digital systems**(25): Digital synthesis workflow, TCL scripting for synopsys design compiler automation, architectural synthesis, scheduling, resource and register sharing, two level synthesis, multilevel synthesis, low power design.
- **Testing**(26): Testing and reliability, design for testability, fault simulation, test pattern generation, ATPG, scan chain design, memory test pattern, BIST, fault tolerant systems.
- **Testing and certification**(24): Measurement instrument certification, instrumentation's metrological confirmation, DAQ boards, digital oscilloscope, logic state analyzer, sensors, conditioning circuits, distributed measurement systems, interconnection bus, reliability analysis, fault classification, fault models.

2009-2012 **First Level Degree (Bachelor) in Electronics, Informatics and Telecommunications Engineering**, *Seconda facoltà di ingegneria con sede a Cesena - University of Bologna*, Cesena, Italy.
Thesis title: Implementation of low latency UDP communication through Ethernet module for FPGA and prototype PCB design.
PDF link

2004-2009 **Electronic and Telecommunications Technician**, *I.T.I.S. Leonardo da Vinci*, Rimini, Italy.
Italian high school diploma

## Personal and Academic Projects

September 2014 **Collision Avoidance**.
Documentation link, GitHub link

June 2014 **Multithreaded Blowfish Algorithm Implementation**.
Documentation link, GitHub link

May 2014 **Porting of nRF24L01P driver to PIC18F**.
Driver of nRF24L01P chip for PIC18F (XC8 compiler) ported from mbed.org
GitHub link

April 2014 **IoT - PicHomeAutomation**.
Four relays and a temperature sensor remotely controlled.
Documentation link, Youtube link, GitHub link

March 2014 **Profiling OpenCV 3 using gprof**.
Documentation link

February 2014 **Design of a 4-state ACS with SystemC**.
An ACS is one of the basic blocks of the Viterbi Algorithm.
- ACS implementation
- SystemC simulation
- Modelsim SystemC simulation
- Modelsim mixed SystemC-Verilog simulation using a given implementation of the ACS and comparation

Documentation link

February 2014 **ASIP design based on Transport Triggered Architecture using TCE**.
Documentation link

February 2014 **FIR ASIC Implementation**.
From Matlab to ASIC implementation and simulation.
- FIR coefficient synthesis with matlab and spectral analysis
- VHDL implementation
- Testbench implementation
- Simulation with Modelsim
- Logic synthesis with Synopsys Design Compiler
- Switching activity-based power consumption estimation
- ASIC Place&Route
- Post Place&Route simulation and switching activity-based power consumption estimation

Documentation link

January 2014 **Temperature Acquisition System**.
Hardware and software design for a temperature acquisition system.

November 2013 **Stepped impedance RF low-pass filter**.
Documentation link

October 2013 **LeapHID**.
Software written in C++ that convert Leap Motion gestures into mouse and keyboard events.
GitHub link

July 2013 **Pipelined DLX Implementation**.
Pipelined implementation of a subset of the DLX instruction set.
Documentation link, GitHub link

June 2013 **DualVth TCL function for Synopsys PrimeTime**.
Script to apply in a smart way the Dual-Vth low power technique on Synopsys PrimeTime.
GitHub link

January 2013 **Parallelization of an MJPEG encoder using OpenMP**.
- GProf profiling
- Parallelization using OpenMP
- Achieved speedup: 2.34 times

January 2013 **Software UART implementation for Nios2 CPU**.
GitHub link

## Working Experience

Jan 2019 - Present **Senior Hardware Design Engineer**, *Arm*, Cambridge, UK.
System Hardware - Reference systems development

Oct 2018 - Dec 2018 **Senior Hardware Design Engineer**, *Arm*, Cambridge, UK.
System Hardware - Power & Clock Architecture Safety

Aug 2018 - Sep 2018 **Hardware Design Engineer**, *Arm*, Cambridge, UK.
System Hardware - Power & Clock Architecture Safety

Aug 2017 - Jul 2018 **Hardware Design Engineer**, *Arm*, Cambridge, UK.
System Hardware - Security & Safety Architecture

Apr 2017 - Jul 2017 **Hardware Design Engineer**, *Arm*, Cambridge, UK.
System Hardware - Security: responsible for integration of the Root of Trust and cryptografic accelerator in systems for different target markets

Sep 2016 - Mar 2017 **Graduate Hardware Design Engineer**, *Arm*, Cambridge, UK.
System Hardware - Security: responsible for integration of the Root of Trust and cryptografic accelerator in systems for different target markets

Sep 2015 - Aug 2016 **Graduate Hardware Design Engineer**, *Arm*, Cambridge, UK.
System Hardware Design: involved in the creation of an entire system with all Arm IPs

Winter 2008 **Freelance Designer**, Rimini, Italy.
Designed and built an automatic commutation device for Paine s.n.c as freelance designer.

Summer 2008 **Electrician**, *Eurotec s.r.l.*, Rimini, Italy.
Industrial plants electrician.

Summer 2007 **Installer**, *Paine s.n.c.*, Rimini, Italy.
Naval electronic devices installer.

Winter 2007 **Internship**, *Protec*, Rimini, Italy.
I spent two week in a PCB assemble company where I acquired PCB soldering ability.

## Interests and Hobbies

Technology, Electronics, Informatics, Embedded Systems, Digital Design, Parallel Computing, Networking, System Administration, IT security, Photography, Music, Science, Physics, Snowboarding, Skateboarding, Swimming, Motorbikes, Cooking